PM-7524

CMOS 8-BIT BUFFERED MULTIPLYING D/A CONVERTER

PMI®

Precision Monolithics Inc.

FEATURES

- ±1/8 LSB Maximum Nonlinearity Over Temperature
- ±0.002 LSB Maximum Zero-Scale Error (I_{LKG} 10nA)
- ±1 LSB Maximum Gain Error Over Temperature
- Microprocessor Compatible
- Improved Resistance to ESD
- Latch-up Resistant; No Schottky Diodes Required
- 5mW @ +5V Maximum Power Consumption
- Available in Die Form

APPLICATIONS

- Microprocessor Controlled Circuits
- Precision AGC Circuits
- Bus Structured Instruments
- Function Generators
- Digitally Controlled Attenuators and Power Supplies

ORDERING INFORMATION †

		PACKAGE		
NON-LINEARITY V_{DD} = +15V	GAIN ERROR	MILITARY* TEMPERATURE −55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/8 LSB	±1 LSB	PM7524AQ	PM7524EQ	PM7524GP
±1/4 LSB	±1.5 LSB	PM7524BQ	PM7524FQ	–
±1/4 LSB	±1.5 LSB	PM7524BRC/883	PM7524FPC	–
±1/4 LSB	±1.5 LSB	–	PM7524FS	–
±1/4 LSB	±1.5 LSB	–	PM7524FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

GENERAL DESCRIPTION

The PM-7524 is an 8-bit monolithic multiplying digital-to-analog converter with input latches. It is compatible with all popular 8-bit microprocessors including the 6800, 8080, 8085, and Z80. Its load cycle is similar to that of a RAM's write cycle.

PMI's tightly controlled thin-film resistor processing provides 1/8 LSB linearity without laser trimming. The design incorporates a matching MOS transistor switch in series with the R-2R ladder terminating resistor and output op amp's feedback resistor. This allows the DAC to achieve an excellent gain tempco and improved power supply rejection.

The PM-7524 exhibits excellent performance on a single +5V to +15V power supply. It is TTL compatible at +5V and dissipates less than 50mW; using 0V or V_{DD} at the digital inputs, the device dissipates less than 50μW at +5V and 150μW at +15V. At +15V it is CMOS compatible.

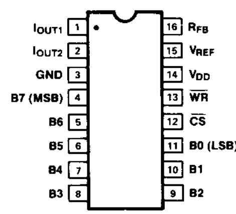
PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

The PM-7524 is manufactured using thin-film resistors on an advanced oxide-isolated silicon-gate CMOS process.

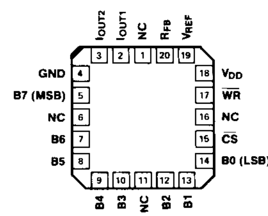
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7524AQ	AD7524UD	
PM7524BQ	AD7524TD	MIL
PM7524BQ	AD7524SD	
PM7524EQ	AD7524CD	
PM7524FQ	AD7524BD	IND
PM7524FQ	AD7524AD	
PM7524GP	AD7524LN	
PM7524FP	AD7524KN	COM
PM7524FPC	AD7524KP	

PIN CONNECTIONS

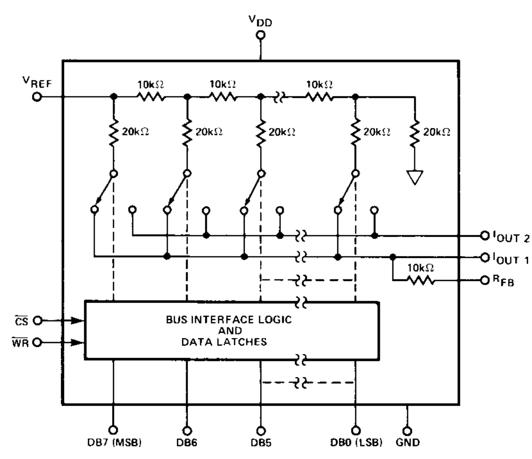


16-PIN EPOXY DIP
(P-Suffix)
16-PIN HERMETIC DIP
(Q-Suffix)
16-PIN SO
(S-Suffix)



20-CONTACT PLCC
(PC-Suffix)
20-CONTACT LCC
(BRC-Suffix)

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} (to GND) .... –0.3V, +17V
V_{REF} (to GND) .... ±25V
R_{FB} (to GND) .... ±25V
Digital Input Voltage to GND .... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) .... –0.3V to V_{DD}
Operating Temperature Range
  Military (AQ, BQ, BRC Versions) .... –55°C to +125°C
  Industrial (EQ, FQ, FP, FPC, FS Versions) . –40°C to +85°C
  Commercial (GP Version) .... 0°C to +70°C
Junction Temperature .... +150°C
Storage Temperature .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (TC)	98	38	°C/W
16-Pin SO (S)	111	35	°C/W
20-Contact PLCC (PC)	76	36	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; Limits apply to the Full Temperature Range for each grade shown: T_A = –55°C to +125°C apply for PM-7524AQ/BQ/ARC/BRC; T_A = –40°C to +85°C apply for PM-7524EQ/FQ/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7524GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7524 MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		—	—	8	Bits
Relative Accuracy (Notes 1, 2)	INL	V_{DD} = +5V PM-7524A/E/G	—	—	±0.1	%FSR
			—	—	(±1/4)	(LSB)
		PM-7524B/F	—	—	±0.2	%FSR
			—	—	(±1/2)	(LSB)
		V_{DD} = +15V PM-7524A/E/G	—	—	±0.05	%FSR
			—	—	(±1/8)	(LSB)
		PM-7524B/F	—	—	±0.1	%FSR
			—	—	(±1/4)	(LSB)
Gain Error (Note 3)	G_{FSE}	V_{DD} = +5V PM-7524A/E/G	—	—	±0.4	%FSR
			—	—	(±1)	(LSB)
		PM-7524B/F	—	—	±0.8	%FSR
			—	—	(±2)	(LSB)
		V_{DD} = +15V T_A = +25°C	—	—	±0.4	%FSR
			—	—	(±1)	(LSB)
		T_A = Full Temp. Range	—	—	±0.6	%FSR
			—	—	(±1.5)	(LSB)
Gain T.C. (Notes 4, 5)	TCG_{FS}		—	±0.001	—	%FSR/°C
DC Power Supply Rejection ($\Delta Gain/\Delta V_{DD}$) (Notes 3, 6)	PSR		—	0.002	0.01	%FSR/%
Output Leakage Current (I_{OUT1}, I_{OUT2}) (Notes 7, 8)	I_{LKG}	T_A = +25°C, V_{DD} = +5V, +15V	—	—	10	
		T_A = Full Temp. Range V_{DD} = +5V	—	—	200	nA
		V_{DD} = +15V	—	—	100	
REFERENCE INPUT						
Input Resistance (Pin 15 to GND) (Note 11)	R_{IN}		7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; Limits apply to the Full Temperature Range for each grade shown: T_A = −55°C to +125°C apply for PM-7524AQ/BQ/ARC/BRC; T_A = −40°C to +85°C apply for PM-7524EQ/FQ/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7524GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7524 MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current (Digital Inputs = X)	I_{DD}	X = V_{IL} or V_{IH}	—	—	1	mA
		X = 0V or V_{DD}				
		T_A = 25°C	—	—	10	μA
		T_A = Full Temp. Range	—	—	25	
ANALOG OUTPUTS						
Output Capacitance (Note 4)	C_O	DB0–DB7 = V_{DD} (Note 12)				
		C_{OUT1} (Pin 1)	—	—	120	pF
		C_{OUT2} (Pin 2)	—	—	30	
		DB0–DB7 = 0V (Note 13)				
		C_{OUT1}	—	—	30	pF
		C_{OUT2}	—	—	120	
DIGITAL INPUTS						
Digital Inputs High	V_{IH}	V_{DD} = +5V	+2.4	—	—	V
		V_{DD} = +15V	+13.5	—	—	
Digital Inputs Low	V_{IL}	V_{DD} = +5V	—	—	+0.8	V
		V_{DD} = +15V	—	—	+1.5	
Input Current (V_{IN} = 0V or V_{DD})	I_{IN}	T_A = 25°C	—	—	±1	μA
		T_A = Full Temp. Range	—	—	±10	
Input Capacitance (V_{IN} = 0V) (Note 4)	C_{IN}	DB0–DB7	—	—	5	pF
		$\overline{WR}$, $\overline{CS}$	—	—	20	
SWITCHING CHARACTERISTICS (Notes 4, 14)						
Chip Select to Write Setup Time ($t_{WR} = t_{CS}$) (Note 14)	t_{CS}	V_{DD} = +5V				
		T_A = +25°C	170	—	—	nA
		T_A = Full Temp. Range				
		PM-7524A/B	240	—	—	
		PM-7524E/F/G	220	—	—	
		V_{DD} = +15V				
		T_A = +25°C	100	—	—	nA
		T_A = Full Temp. Range				
		PM-7524A/B	150	—	—	
		PM-7524E/F/G	130	—	—	
Chip Select to Write Hold Time	t_{CH}		0	—	—	ns
Write Pulse Width ($t_{CH} \geq t_{WR}$, $t_{CH} \geq 0$)	t_{WR}	V_{DD} = +5V				
		T_A = +25°C	150	—	—	ns
		T_A = Full Temp. Range				
		PM-7524A/B	220	—	—	
		PM-7524E/F/G	200	—	—	
		V_{DD} = +15V				
		T_A = +25°C	100	—	—	ns
		T_A = Full Temp. Range				
		PM-7524A/B	150	—	—	
		PM-7524E/F/G	130	—	—	

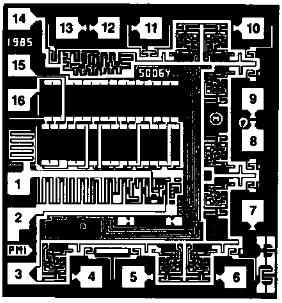
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; Limits apply to the Full Temperature Range for each grade shown: T_A = −55°C to +125°C apply for PM-7524AQ/BQ/ARC/BRC; T_A = −40°C to +85°C apply for PM-7524EQ/FQ/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7524GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7524 MIN	TYP	MAX	UNITS
Data Setup Time	t_{DS}	V_{DD} = +5V				
		T_A = +25°V	135	—	—	ns
		T_A = Full Temp. Range	170	—	—	
		V_{DD} = +15V				
		T_A = +25°C	60	—	—	
		T_A = Full Temp. Range				ns
		PM-7524A/B	100	—	—	
		PM-7524E/F/G	80	—	—	
Data Hold Time	t_{DH}		10	—	—	ns
DYNAMIC PERFORMANCE						
Propagation Delay (From Digital Input to 90% of Final Analog Output Current) (Notes 4, 9)	t_{PD}	V_{DD} = +5V				
		T_A = +25°C	—	—	150	
		T_A = Full Temp. Range				ns
		PM-7524A/B	—	—	200	
		PM-7524E/F/G	—	—	175	
		V_{DD} = +15V				
		T_A = +25°C	—	—	65	ns
		T_A = Full Temp. Range				
		PM-7524A/B	—	—	90	
Output Current Settling Time (To 1/2 LSB) (Notes 4, 9, 15)	t_S	V_{DD} = +5V				
		T_A = +25°C	—	—	300	
		T_A = Full Temp. Range	—	—	350	ns
		V_{DD} = +15V				
		T_A = +25°C	—	—	200	
		T_A = Full Temp. Range	—	—	250	
AC Feedthrough I_{OUT1}, I_{OUT2} (Note 4)	FT		—	—	0.25	%FSR
Digital Charge Injection (Note 16)	Q	V_{DD} = +5V, T_A = +25°C	—	50	—	nV/s
		V_{DD} = +15V, T_A = +25°C	—	55	—	

NOTES:

1. Guaranteed monotonic over full temperature range and at V_{DD} = +5V and +15V.
2. FSR (Full Scale Range) = V_{REF} − 1LSB.
3. Using internal feedback resistor.
4. Guaranteed by design and not production tested.
5. Gain TC measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
6. ΔV_{DD} = ±10%.
7. DB0−DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT1}.
8. DB0−DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT2}.
9. I_{OUT1} load = 100Ω; C_{EXT} = 13pF; $\overline{WR}$ = $\overline{CS}$ = 0V; DB0−DB7 = 0V to V_{DD} or V_{DD} to 0V.
10. V_{REF} = ±10V, f = 100kHz; DB0−DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V.
11. Temperature coefficient approximately equals +50ppm/°C.
12. DB0−DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V.
13. DB0−DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V.
14. See Timing Diagram.
15. Extrapolated: t_S (1/2 LSB) = t_{PD} + 6.2τ, where τ = the measured first time constant of the final RC decay.
16. V_{REF} = 0V; Digital Inputs = 0V to V_{DD}.

DICE CHARACTERISTICS



DIE SIZE 0.070 × 0.076 inch, 5320 sq. mils
(1.78 × 1.93 mm, 3.43 sq. mm)

1. I_{OUT1}
2. I_{OUT2}
3. GND
4. DB7 (MSB)
5. DB6
6. DB5
7. DB4
8. DB3
9. DB2
10. DB1
11. DB0 (LSB)
12. $\overline{CS}$
13. $\overline{WR}$
14. V_{DD}
15. V_{REF}
16. R_{FB}

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at V_{DD} = +5V and +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = +25°C.

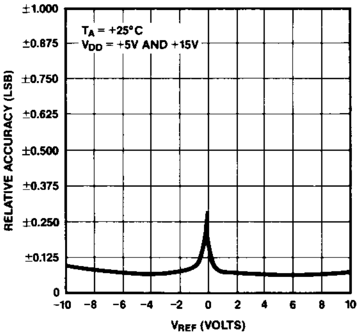
PARAMETER	SYMBOL	CONDITIONS	PM-7524G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Relative Accuracy (Notes 1, 2)	INL	V_{DD} = +5V	±0.2 (±1/2)	%FSR (LSB) MAX
		V_{DD} = +15V	±0.1 (±1/4)	%FSR (LSB) MAX
Gain Error (Note 3)	G_{FSE}	V_{DD} = +5V	±0.8 (±2)	%FSR (LSB) MAX
		V_{DD} = +15V	±0.4 (±1)	%FSR (LSB) MAX
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$) (Notes 3, 4)	PSRR		0.01	%FSR/% MAX
Output Leakage Current (I_{OUT1}, I_{OUT2}) (Notes 5, 6)	I_{LKG}		10	nA MAX
REFERENCE INPUT				
Input Resistance	R_{IN}	(Note 7)	7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Inputs High	V_{IH}	V_{DD} = +5V V_{DD} = +15V	+2.4 +13.5	V MIN
Digital Inputs Low	V_{IL}	V_{DD} = +5V V_{DD} = +15V	+0.8 +1.5	V MAX
Input Current (V_{IN} = 0V or V_{DD})	I_{IN}		±1	μA
POWER SUPPLY				
Supply Current (Digital Inputs = X)	I_{DD}	X = V_{IL} or V_{IH}	1	mA
		X = 0V or V_{DD}	10	μA

NOTES:
1. Guaranteed monotonic over full temperature range and at V_{DD} = +5V and +15V.
2. FSR (Full Scale Range) = V_{REF} − 1 LSB.
3. Using internal feedback resistor.
4. ΔV_{DD} = ±10%.
5. DB0–DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT1}.
6. DB0–DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V; V_{REF} = ±10V, for I_{OUT2}.
7. Temperature coefficient approximately equals +50ppm/°C.

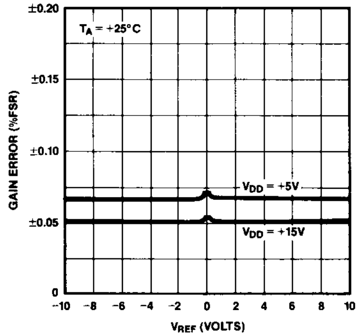
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

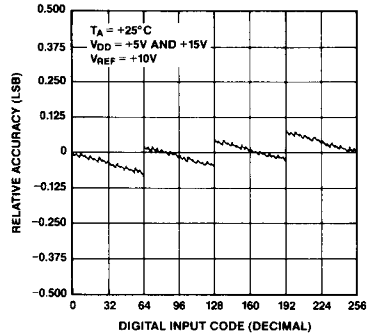
RELATIVE ACCURACY vs REFERENCE VOLTAGE



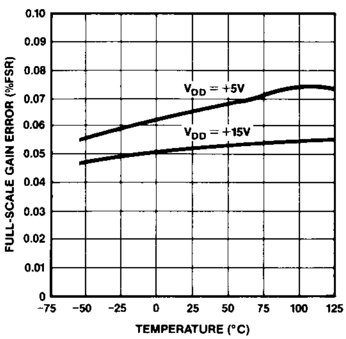
GAIN ERROR vs REFERENCE VOLTAGE



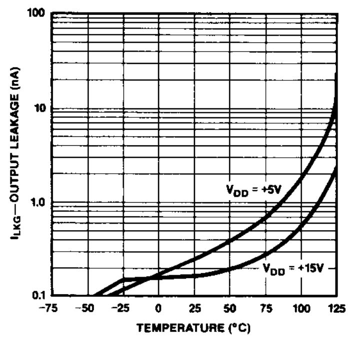
RELATIVE ACCURACY vs DIGITAL INPUT CODE



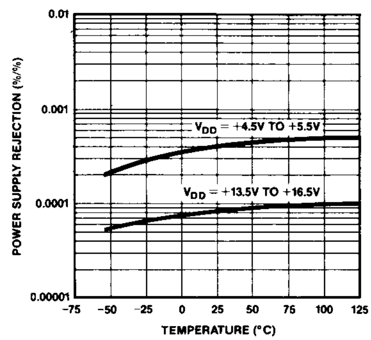
FULL-SCALE GAIN ERROR vs TEMPERATURE



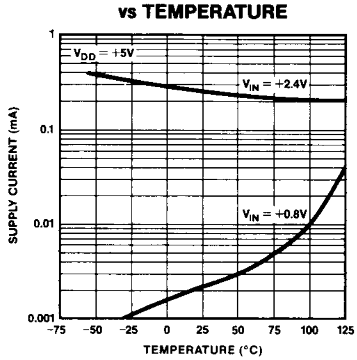
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



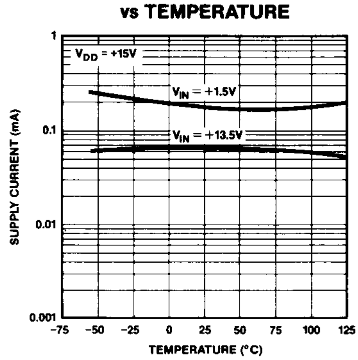
POWER SUPPLY REJECTION vs TEMPERATURE



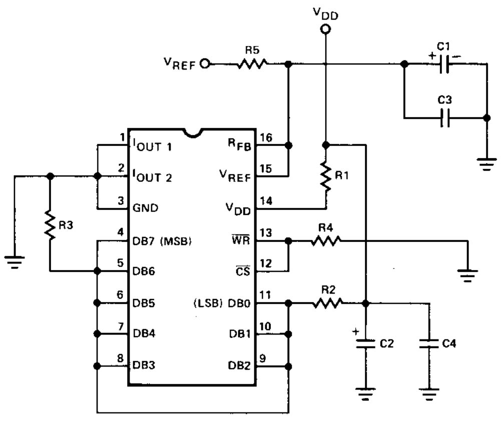
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



BURN-IN CIRCUIT



NOTES:
1. C1 = C2 = 4.7μF TANTALUM 50V EVERY 10th DEVICE.
2. C3 = C4 = 0.01μF CERAMIC 50V EVERY 10th DEVICE.

DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

PROPAGATION DELAY

The time for the output current to reach 90% of its final value from a given digital input signal.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideal output is equal to V_{REF} - 1 LSB.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE

Capacitance from $I_{OUT\,1}$ and $I_{OUT\,2}$ terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on $I_{OUT\,1}$ terminal with all digital inputs low or on $I_{OUT\,2}$ terminal when all inputs are high.

CIRCUIT DESCRIPTION

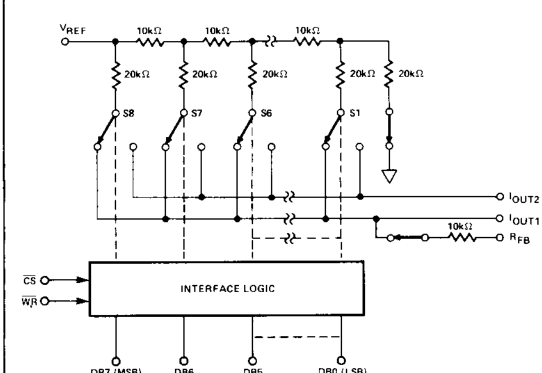
CIRCUIT INFORMATION

The PM-7524 is an 8-bit multiplying CMOS digital-to-analog converter with on-board data latches. It is fabricated using a highly stable thin-film R-2R resistor ladder network and eight N-channel current switches. A voltage or current reference and an operational amplifier are all that is required in the majority of applications.

Figure 1 shows a simplified circuit of the PM-7524 converter. The R-2R ladder, current steering switches, and interface logic are shown. The switches are binarily weighted and switch the ladder current between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines; this switching allows a constant current to be maintained in each resistor leg regardless of the switch state.

The simplified circuit of Figure 1 also shows the matching switches in series with the ladder terminating and R_{FB} (feedback) resistors. These switches are designed to temperature-track the ladder current-steering switches and improve power supply rejection. Both switches are MOS transistors that have their gate turn-on voltage derived from V_{DD} supply. This means the terminating and feedback resistors are open-circuit when V_{DD} power is off. If R_{FB} is used as part of an op amp's feedback element, and the op amp's supply comes on before the DAC, the op amp's output will go to the rails. It remains in this open-loop condition until the DAC's V_{DD} is applied. In applications where the op amp's supply must come on before the DAC, a voltage clamp or external feedback resistor may be necessary.

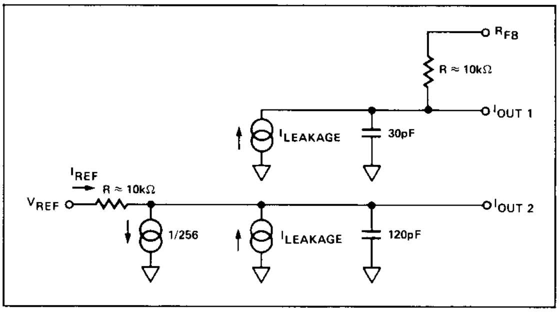
FIGURE 1: PM-7524 Functional Diagram



EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an equivalent circuit for the PM-7524 with all digital inputs LOW. The $I_{OUT\ 1}$ and $I_{OUT\ 2}$ leakage current source is the combination of surface and junction leakages to the substrate. The 1/256 current source represents the constant 1-bit current drain through the ladder termination resistor. The situation is reversed with all digital inputs HIGH, i.e., the current output is now switched to the $I_{OUT\ 1}$ terminal. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

FIGURE 2: PM-7524 Equivalent Circuit (All Digital Inputs LOW)



INTERFACE LOGIC

MODE SELECTION

The mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

The PM-7524 is in the WRITE mode when both the $\overline{CS}$ and $\overline{WR}$ are both LOW; the input latches are transparent and the output immediately follows the data input logic. See the MODE SELECTION TABLE.

MODE SELECTION TABLE

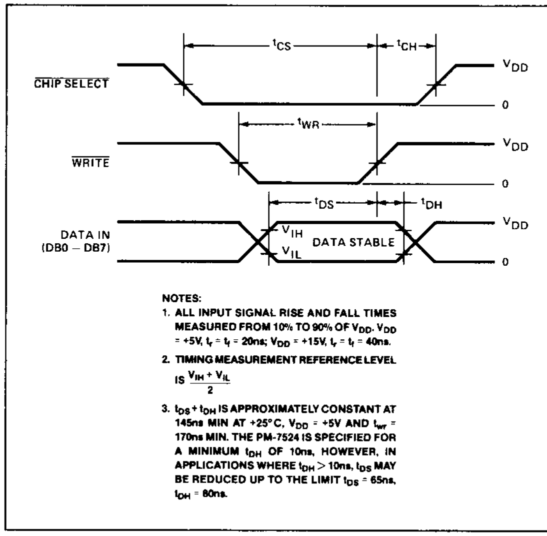
$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB0—DB7) inputs (transparent)
H	X	HOLD	Data bus (DB0—DB7) is locked out
X	H	HOLD	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumes a HIGH state

L = Low State, H = High State, X = Don't Care.

HOLD MODE

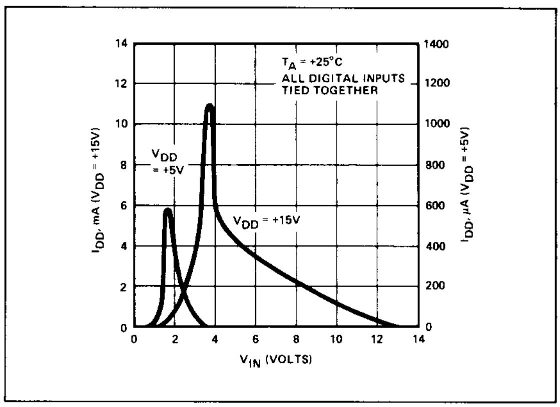
The MODE SELECTION TABLE shows the output results when either $\overline{CS}$ or $\overline{WR}$ is HIGH. The output holds the value corresponding to the last digital inputs prior to $\overline{CS}$ or $\overline{WR}$ assuming the HIGH state.

WRITE CYCLE TIMING DIAGRAM



Supply current (I_{DD}) versus Logic input voltage (V_{IN}) is shown in Figure 3. This plot shows the supply current for both V_{DD} = +5V and V_{DD} = +15V.

FIGURE 3: Supply Current vs Logic Level



APPLICATIONS

FIGURE 4: Unipolar Binary Operation (2-Quadrant Multiplication)

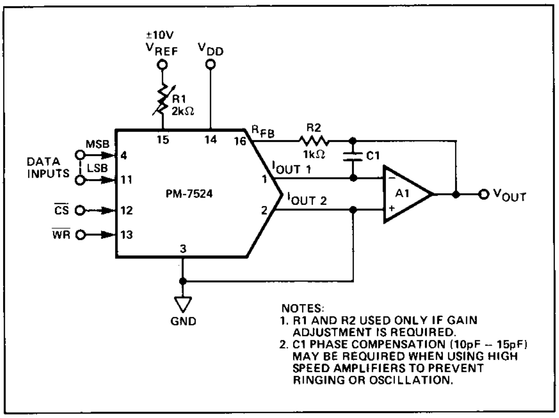


TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB … LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

NOTE:
$1\text{LSB} = (2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB … LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right)$

NOTE:
$1\text{LSB} = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

FIGURE 6: PM-7524/8085A Interface

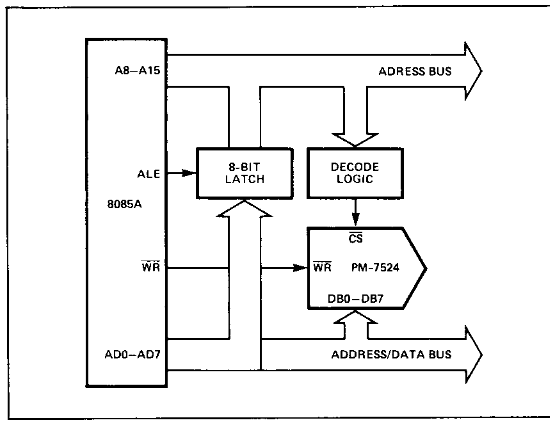


FIGURE 5: Bipolar (4-Quadrant) Operation

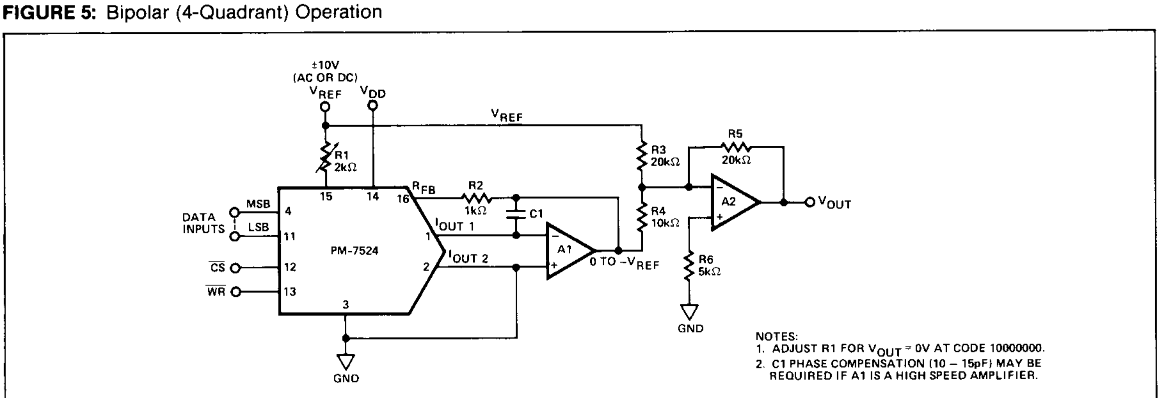


FIGURE 7: PM-7524/MC6800 Interface

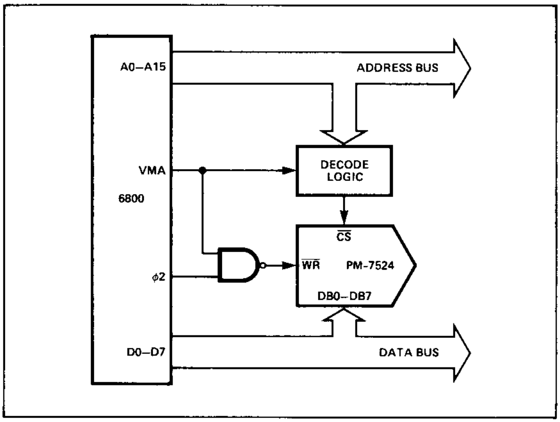
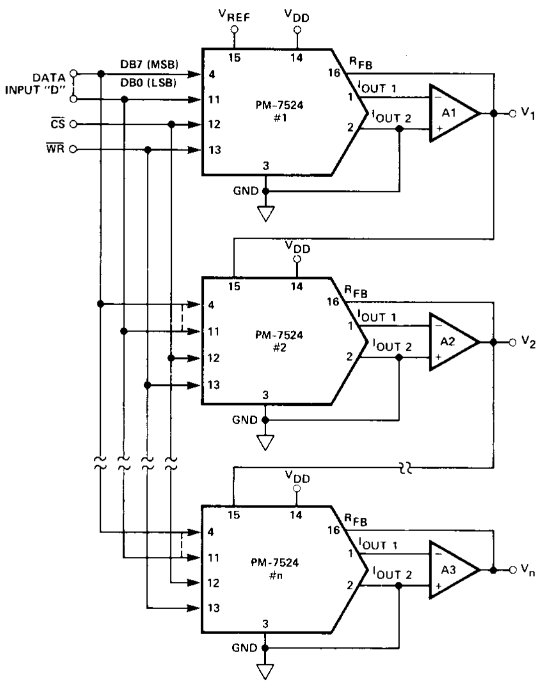


FIGURE 8: Power Generation Connection



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$
$V_2 = +(V_{REF})(D^2)$
$V_n = -(V_{REF})(D^n)$, n AN ODD INTEGER
$V_n = +(V_{REF})(D^n)$, n AN EVEN INTEGER

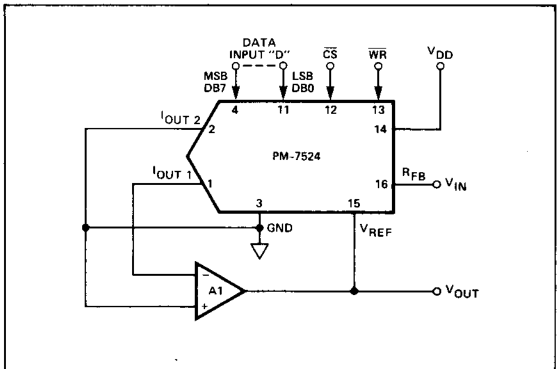
WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \cdots \frac{DB0}{2^8}$$

AND

DB_n = 1 or 0

FIGURE 9: Divider (Digitally Controlled Gain)



EQUATIONS

$$V_{OUT} = \frac{-V_{IN}}{D}$$

$$A_V = \frac{-V_{OUT}}{V_{IN}} = -\frac{1}{D}$$ WHERE: A_V = VOLTAGE GAIN

AND WHERE:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \cdots \frac{DB0}{2^8}$$

DB_N = 1 or 0

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)
D = 00000001, $A_V = -256$
D = 10000000, $A_V = -\frac{256}{128} = -2$
D = 11111111, $A_V = -\frac{256}{255}$